VERIFICATION OF TRANSLATION

I, Jin-Seok Kim of 1-170, Soonhwa-Dong, Jung-Gu, Seoul, Republic of Korea, hereby declare that, to the best of my knowledge and belief, the attached is a true English translation of the certified copy of the Korean Patent Application No. 2000-85582.

Signature of translator

Jin Seok Kim

Dated this 29th day of January, 2003

(Translation)

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Application Number: Patent Application No. 2000-85582

Date of Application: December 29, 2000

Applicant(s): HYNIX SEMICONDUCTOR INC.

COMMISSIONER

[ABSTRACT]

[Summary]

The present invention discloses a method for forming a metal gate capable of preventing degradation in a characteristic of a gate insulating film upon formation of the metal gate. The method of forming the metal gate comprises the steps of providing a silicon substrate having device isolation films of a trench shape for defining an active region; forming a gate insulating film on the surface of the silicon substrate by means of thermal oxidization process; sequentially forming a barrier metal film and a metal film for gate on the gate insulating film; and patterning the metal film for gate, the barrier metal film and the gate insulating film, wherein deposition of the barrier metal film and the metal film for gate is performed by means of atomic layer deposition (ALD) process or remote plasma chemical vapor deposition (CVD) process.

[Representative Drawing]

Fig. 3C

[SPECIFICATION]

[Title of the Invention]

METHOD FOR FORMING METAL GATE OF SEMICONDUCTOR DEVICE

[Brief Description of the Drawings]

Figs. 1a and 1b are graphs illustrating accumulated capacity(F) – voltage(V) curves in case of directly depositing TiN or WN film and a tungsten(W) film on a silicon oxide film by means of sputtering according to a conventional technology;

Figs. 2a through 2c are graphs illustrating accumulated capacity(F) – voltage(V) curves in a TiN metal gate deposited in a thermal deposition method of $TiCl_4$+NH_3 at 650°C according to a conventional technology; and

Figs. 3a through 3c are cross-sectional views of semiconductor devices for explaining a method of forming a metal gate according to one embodiment of the present invention.

<the Reference Numerals in the Drawings>

1: silicon substrate 2: device isolation film

3: gate insulating film 4: barrier metal film

5: metal film for gate 6: hard mask film

10: metal gate

[Detailed Description of the Invention]

[Object of the Invention]

[Technological Background of the Invention and Description of the Prior Art]

The invention relates generally to a method of forming a metal gate in semiconductor devices. More particularly, the present invention relates to a method of forming a metal gate in semiconductor device capable of preventing degradation of a characteristic in a gate insulating film.

As noted well, a silicon oxide film(SiO_2) has been mainly used as a material of a gate insulating film in MOSFET and a polysilicon film has used as a material of gate. As the integration level of the semiconductor devices becomes higher, however, it is required that the line width of the gate and the thickness of the gate insulating film be reduced. In case that a silicon oxide film is used as the material of the gate insulating film, if the thickness of the gate insulating film is too thinner, a device characteristic is not stable since the leakage current due to a direct tunneling through the gate insulating film becomes greater.

For example, when the silicon oxide film as the gate insulating film of DRAM and logic devices currently manufactured in mass production is applied to a 70mm technology device, it is expected that its thickness will be 30 - 35Å in DRAM and be 13 - 15Å in logic devices. As the capacitor component increased by a gate poly depletion is increased to be 3 - 8 Å, however, it is difficult to reduce the electrical thickness (Teff) occupied by a gate oxide film of 15 - 30 Å.

Therefore, as one method to overcome the above problem, there has been recently an effort to use a high dielectric material having a relatively higher dielectric constant than a silicon oxide film as the material of the gate insulating film. Also, in order to

minimize the poly gate depletion, there has been an effort to use a metal gate instead of the poly gate.

In case of the metal gate, TiN or WN film as a barrier metal film is intervened between the metal film for gate and the gate insulating film and a hard mask film used as an etch mask is positioned on the metal film for gate.

[Technical Means for Achieving the Object of the Invention]

However, in case of forming a metal gate on a gate insulating film of a silicon oxide film according to a conventional technology, there is a problem that a characteristic of the gate insulating film is degraded as follows.

Deposition of a metal film for gate is commonly performed by sputtering or chemical vapor deposition (CVD). At this time, the metal film for gate, specially, in case of directly depositing the barrier metal film on the gate oxide film, the interface characteristic and the insulating characteristic of the gate insulating film can be degraded.

Figs. 1a and 1b are graphs illustrating accumulated capacity(F) – voltage(V) curves of a MOS transistor in case of sequentially directly depositing TiN or WN film as a barrier film and a tungsten(W) film as a metal film gate on a gate insulating film made of a silicon oxide film by means of sputtering according to a conventional technology;

As shown, in case of sequentially depositing the barrier metal film(TiN or WN) and the tungsten film on the gate insulating film made of the silicon oxide film, there occurs an oxide trap charge due to an excessive interface trap density of about 1E12/eV-cm^2 and a hysteresis of about 1E12/cm^2 by means of a hump without significant regard to

the deposition materials (TiN or WN) and sputtering methods (IMP, collimated, conventional) of the accumulated capacity-voltage characteristic, with a subsequent annealing process not performed. Due to this, there are a damage of the gate insulating itself and a severe damage in the interface with the substrate.

Meanwhile, the damage can be recovered by some degree through high temperature annealing process of 800°C but a complete recover of the damaged gate insulating film could not be expected. In particular, there are disadvantages that a high temperature annealing process must be performed and the electrical thickness (Teff) of the gate insulating film is increased.

Figs. 2a through 2c are graphs illustrating accumulated capacity(F) – voltage(V) curves in the TiN metal gate deposited in a thermal deposition method of $TiCl_4$+NH_3 at 650°C.

As shown, the MOS transistor characteristic after deposition is relatively better than that deposited by sputtering method. However, degradation of the gate oxide integrity (GOI) characteristic is caused due to an increase of the electrical thickness (Teff) and the oxide film trap charge in the gate insulating film after a subsequent annealing process, that is, increased hysteresis. Particularly, severe degradation of the characteristic can be caused when the MOS transistor is manufactured.

Therefore, the present invention is contrived to solve the above problems and an object of the present invention is to provide a method of forming a metal gate capable of preventing degradation in the characteristic of the gate insulating film.

[Structure and Operation of the Invention]

In order to accomplish the above object, a method of forming a metal gate according to the present invention is characterized in that it comprises the steps of providing a silicon substrate having device isolation films of a trench shape for defining an active region; forming a gate insulating film on the surface of the silicon substrate by means of thermal oxidization process; sequentially forming a barrier metal film and a metal film for gate on the gate insulating film; and patterning the metal film for gate, the barrier metal film and the gate insulating film, wherein deposition of the barrier metal film and the metal film for gate is performed by means of atomic layer deposition (ALD) process or remote plasma chemical vapor deposition process.

According to the present invention, the barrier metal film and the metal film for gate are deposited by means of atomic layer deposition (ALD) process or remote plasma CVD process. Thus, damage of the gate insulating film that can be generated during the process of depositing the films can be minimized.

Figs. 3a through 3c are cross-sectional views of semiconductor devices for explaining a method of forming a metal gate according to one embodiment of the present invention.

Referring now to Fig. 3a, a silicon substrate 1 is provided. Device isolation films 2 of a trench shape for defining an active region are formed at given regions of the silicon substrate 1. At this time, the device isolation films 2 may be formed by means of common LOCOS process. A gate insulating film 3 made of a silicon oxide film of 10 –

40Å in thickness is formed on the surface of the silicon substrate 1 by means of thermal oxidization process. At this time, it is preferred that the thermal oxidization process be performed in a furnace of 650 – 900 °C by means of wet (H_2/O_2) or dry (O_2) method.

Meanwhile, a high dielectric constant insulating film of any one of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Zr-silicate, Hf-silicate, La_2O_3, and 3-dimensional mixed insulating films (ZrAlO, HfAlO, $ZrSiO_4$ and $HfSiO_4$) instead of the silicon oxide film by the thermal oxidization process may be formed. Also, before the high dielectric constant insulating film is deposited, an ultra thin silicon oxide film may be formed. Further, in case of using the high dielectric constant insulating film as a gate insulating film, the high dielectric constant insulating film may be experienced by an annealing process using a rapid thermal process under oxygen, nitrogen or inactive atmosphere for 10 – 300 seconds or a furnace process for 10 –100 minutes and may be experienced by UV-ozone process.

In addition, though not shown in the drawing, before the gate insulating film 3 is formed, a capacitor may be formed in a trench structure. At this time, the dielectric film may include one of an ON film, Ta_2O_5 film, an Al_2O_3 film, a BST film and a SBT film.

Referring now to Fig. 3b, a barrier metal film 4 and a metal film 5 for gate are sequentially deposited on the gate insulating film 3. It is preferred that the barrier metal film 4 and the metal film 5 for gate be deposited by means of a deposition process not a high temperature thermal deposition method, for example, atomic layer deposition (ALD) process or remote plasma CVD process with them not affected by metal

penetration or implantation.

In the above, as the ALD process allows deposition by means of cyclic dosing and purging at the temperature of 150 – 350 °C, degradation of the characteristic of the interface between the gate insulating film 3 and the substrate 1 and the gate insulating film 3 itself can be prevented. It is preferred that the ALD process be performed using one of N_2, NH_3 or ND_3 as materials for purging a precursor at the temperature of 50 – 450 °C under the pressure of 0.05 – 3 Torr.

Also, as the remote plasma CVD process forms plasma in remote to deposit a thin film, it can obtain the same effect to the ALD process. It is preferred that the remote plasma CVD process be performed using an electron cyclotron resonance (ECR) as a plasma source and He, Ar, Kr or Xe as a plasma excitation gas under the frequency of 2.0 – 9 GHz. In addition, upon the remote plasma CVD process, a metal source such as Ti into the chamber is sprayed around the wafer and the source of N is excited around the plasma, so that they can be introduced around the wafer.

Meanwhile, the barrier metal film 4 may be formed of one of a group consisting of TiN, TiAlN, TaN, MoN or WN. It is preferred that the thickness of the barrier metal film 4 be 50 – 500 Å. Also, the metal film 5 for gate may be formed of one of a group consisting of W, Ta, Al, TiSix, CoSix and NiSix or may be formed in a stack structure of polysilicon, a tungsten nitride film and a tungsten film. It is preferred that the thickness of the metal film 5 for gate be 300 – 1500 Å. The hard mask film 6 may be formed of a silicon oxide film(SiO_2), a silicon nitride film(Si_3N_4) or silicon oxynitride film(SiON).

The thickness of the hard mask film 6 is 300 – 2000 Å.

In the above, when the barrier metal film, for example, TiN is deposited by means of the remote plasma CVD process, a source of Ti may include $TiCl_4$, TDEAT or TDMAT and a source of N may include N_2, NH_3 or ND_3. Also, in case of depositing TiAlN as the barrier metal film, a source of Ti may include $TiCl_4$, TDEAT or TDMAT, a source of N may include N_2, NH_3 or ND_3 and a source of Al may include $AlCl_3$ or TMA[$Al(CH_3)_3$]. In addition, in case of depositing TaN as the barrier metal film, a source of Ta may include $TaCl_4$ or Ta tert-butaoxide and a source of N may include N_2, NH_3 or ND_3. Also, in case of depositing MoN as the barrier metal film, a source of Mo may include $MoCl_4$, MoF_6 or Mo tert-butaoxide and a source of N may include N_2, NH_3 or ND_3. In addition, in case of depositing WN as the barrier metal film, a source of W may include WF_6 or WCl_4 and a source of N may include N_2, NH_3 or ND_3.

Referring now to Fig. 3c, the hard mask film 6 is patterned by means of common photolithography process. Then, the metal film 5 for gate, the barrier film 4 and the gate insulating film 3 are sequentially etched by means of an etching process using the patterned hard mask film 6 as an etch mask, thus forming a metal gate 10

The metal gate 10 of the present invention, that is formed by the above profess, can prevent degradation in the characteristic of the gate insulating film 3 made of a silicon oxide film since the metal film 5 for gate including the barrier metal film 4 is deposited by means of the ALD process or the remote plasma CVD process.

Meanwhile, the above mentioned embodiment has illustrated the process of

forming the gate by a traditional gate formation process, that is, the process by which the gate insulating film and a conductive film for gate are deposited and are then patterned. However, the present invention can be applied to a damascene process by which after a gate formation region is defined through formation and removal of a sacrifice gate, the metal gate is formed in the gate formation region. More particularly, if the method according to the present invention by which the barrier metal film and the metal film for gate are deposited by the ALD process or the remote plasma CVD process is applied to the gate formation process using the damascene process, a further improved effect can be obtained.

[Effect of the Invention]

As can be understood from the above description, the present invention forms a metal gate, where a barrier metal film and a metal film for gate are deposited by means of ALD process or remote plasma CVD process. Thus, the present invention can prevent degradation in the characteristic of a gate insulating film. Therefore, the present invention can improve not only a characteristic of the metal gate but also a characteristic of a device. Further, as the ALD process and the remote plasma CVD process have a good step coverage, there is an advantage in the process itself and can be advantageously applied in manufacturing high speed/high density devices.

The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional

modifications and applications within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.

[CLAIMS]

[Claim 1]

A method of forming a metal gate in a semiconductor device comprising the steps of:

providing a silicon substrate having device isolation films of a trench shape for defining an active region;

forming a gate insulating film on the surface of said silicon substrate by means of thermal oxidization process;

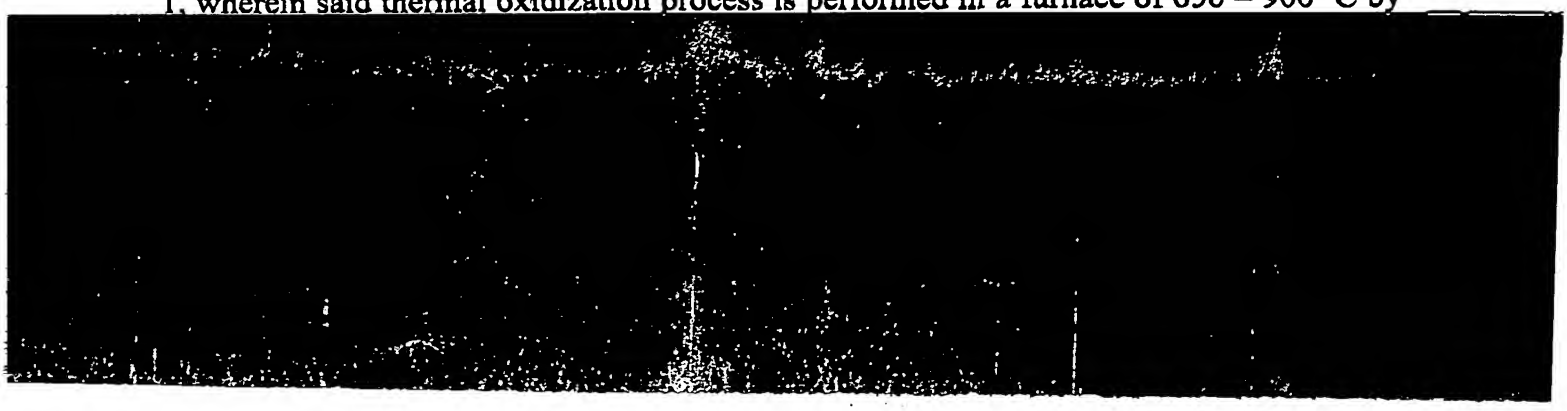
sequentially forming a barrier metal film and a metal film for gate on said gate insulating film; and

patterning said metal film for gate, said barrier metal film and said gate insulating film,

wherein deposition of said barrier metal film and said metal film for gate is performed by means of atomic layer deposition (ALD) process or remote plasma chemical vapor deposition process.

[Claim 2]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said thermal oxidization process is performed in a furnace of 650 – 900 °C by



[Claim 3]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said barrier metal film is one selected from a group consisting of TiN, TiAlN, TaN, MoN and WN.

[Claim 4]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said ALD process is performed using one of N_2, NH_3 or ND_3 as a material for purging a precursor at the temperature of 50 – 450 °C under the pressure of 0.05 – 3 Torr.

[Claim 5]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said remote plasma CVD process is performed using an electron cyclotron resonance (ECR) as a plasma source and He, Ar, Kr or Xe as a plasma excitation gas under the frequency of 2.0 – 9 GHz.

[Claim 6]

The method of forming a metal gate in a semiconductor device according to claim 3, wherein upon deposition of said TiN, a source of Ti includes $TiCl_4$, TDEAT or TDMAT and a source of N include N_2, NH_3 or ND_3.

[Claim 7]

The method of forming a metal gate in a semiconductor device according to claim 3, wherein upon deposition of said TiAlN, a source of Ti includes $TiCl_4$, TDEAT or TDMAT, a source of Al includes $AlCl_3$ or TMA[$Al(CH_3)_3$] and a source of N includes N_2,

NH_3 or ND_3 and.

[Claim 8]

The method of forming a metal gate in a semiconductor device according to claim 3, wherein upon deposition of said TaN, a source of Ta includes $TaCl_4$ or Ta tert-butaoxide and a source of N includes N_2, NH_3 or ND_3.

[Claim 9]

The method of forming a metal gate in a semiconductor device according to claim 3, wherein upon deposition of said MoN, a source of Mo includes $MoCl_4$, MoF_6 or Mo tert-butaoxide and a source of N includes N_2, NH_3 or ND_3.

[Claim 10]

The method of forming a metal gate in a semiconductor device according to claim 3, wherein upon deposition of said WN, a source of W includes WF_6 or WCl_4 and a source of N includes N_2, NH_3 or ND_3.

[Claim 11]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said metal film for gate is one selected from W, Ta, Al, TiSix, CoSix and NiSix.

[Claim 12]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said metal film for gate has a stack structure of polysilicon, a tungsten nitride film and a tungsten film.

[Claim 13]

The method of forming a metal gate in a semiconductor device according to claim 1, wherein said metal film for gate has a stack structure of polysilicon, a tungsten nitride film and a tungsten film.

FIG. 1A (PRIOR ART)

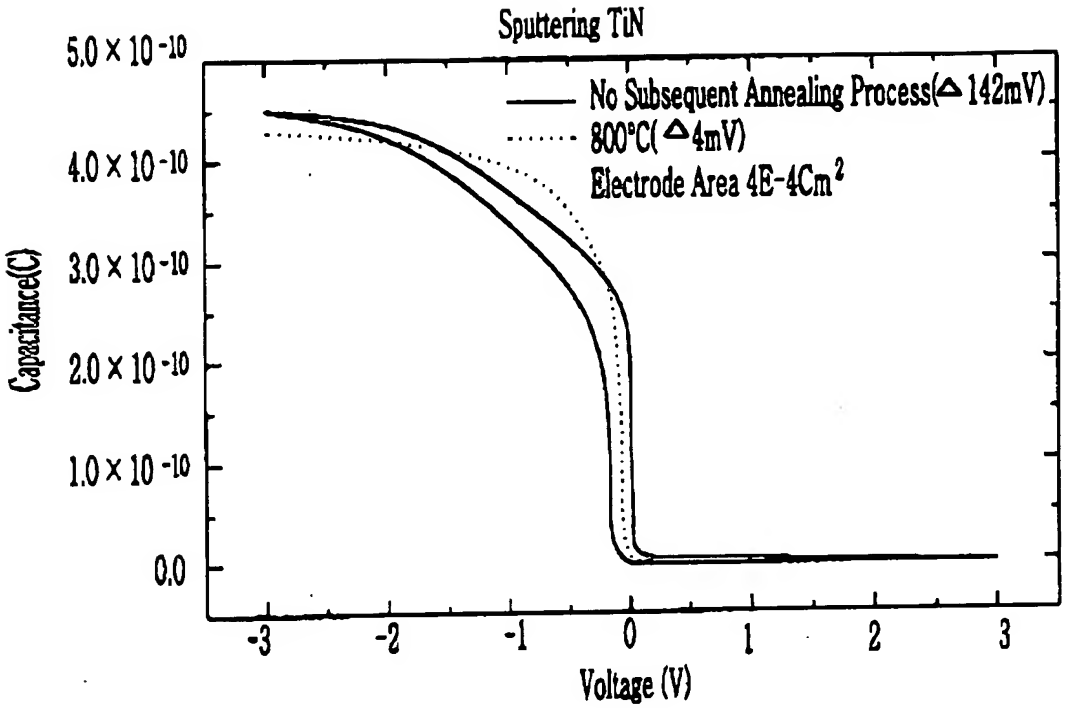


FIG. 1B (PRIOR ART)

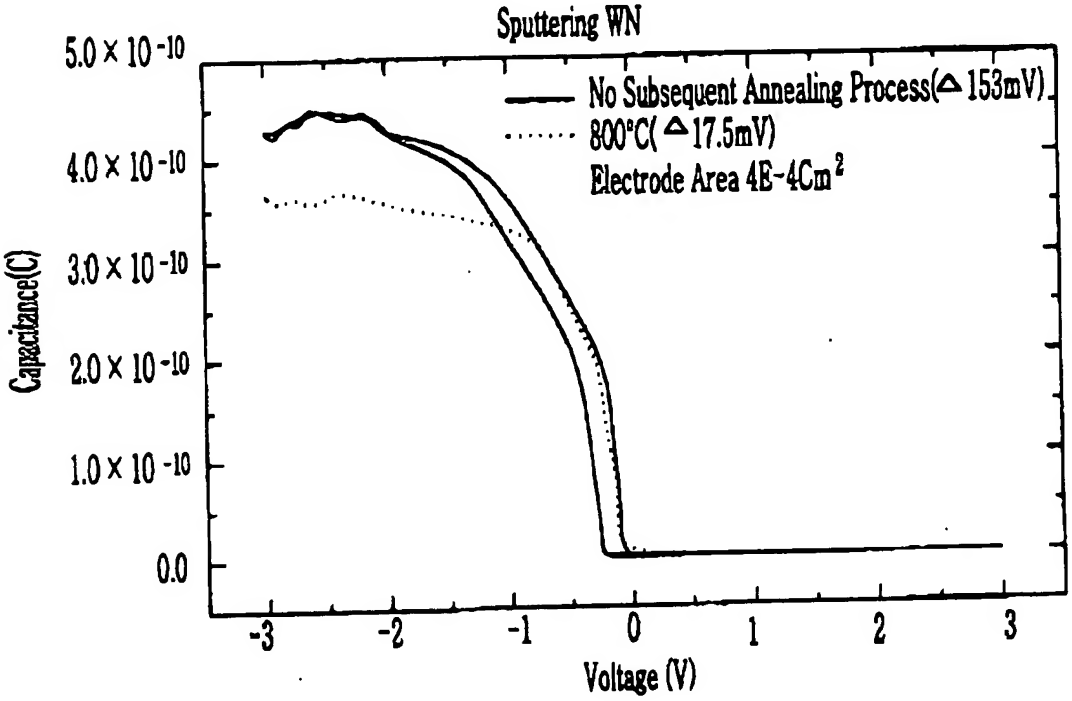


FIG. 2A (PRIOR ART)

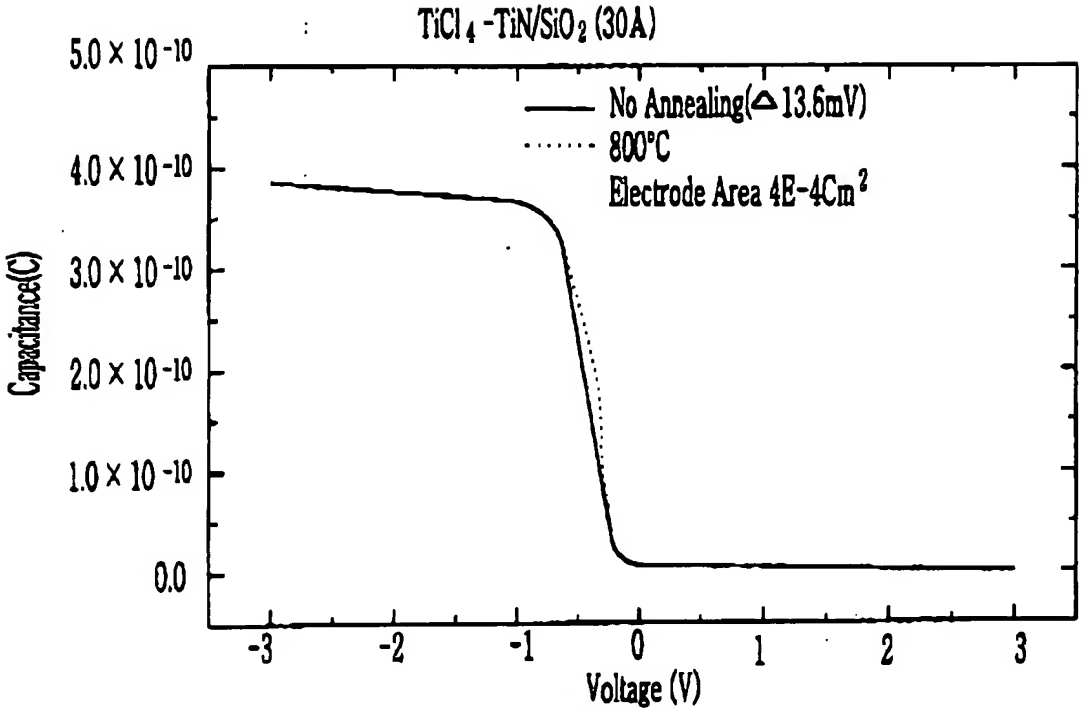


FIG. 2B (PRIOR ART)

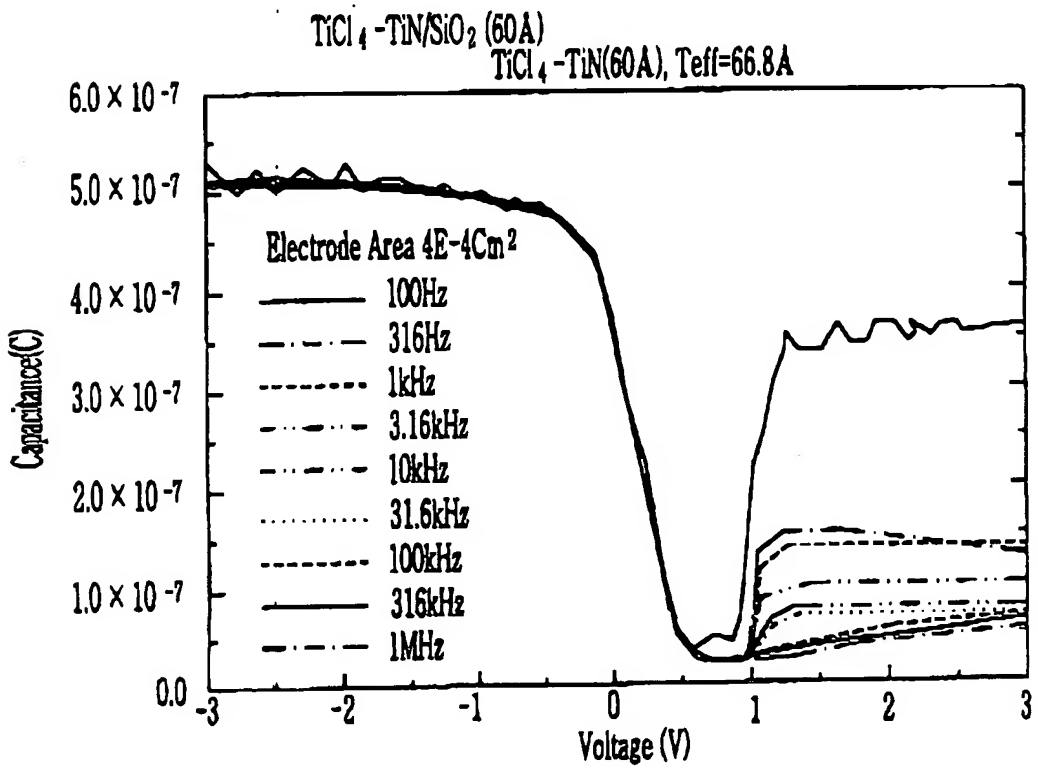


FIG. 2C (PRIOR ART)

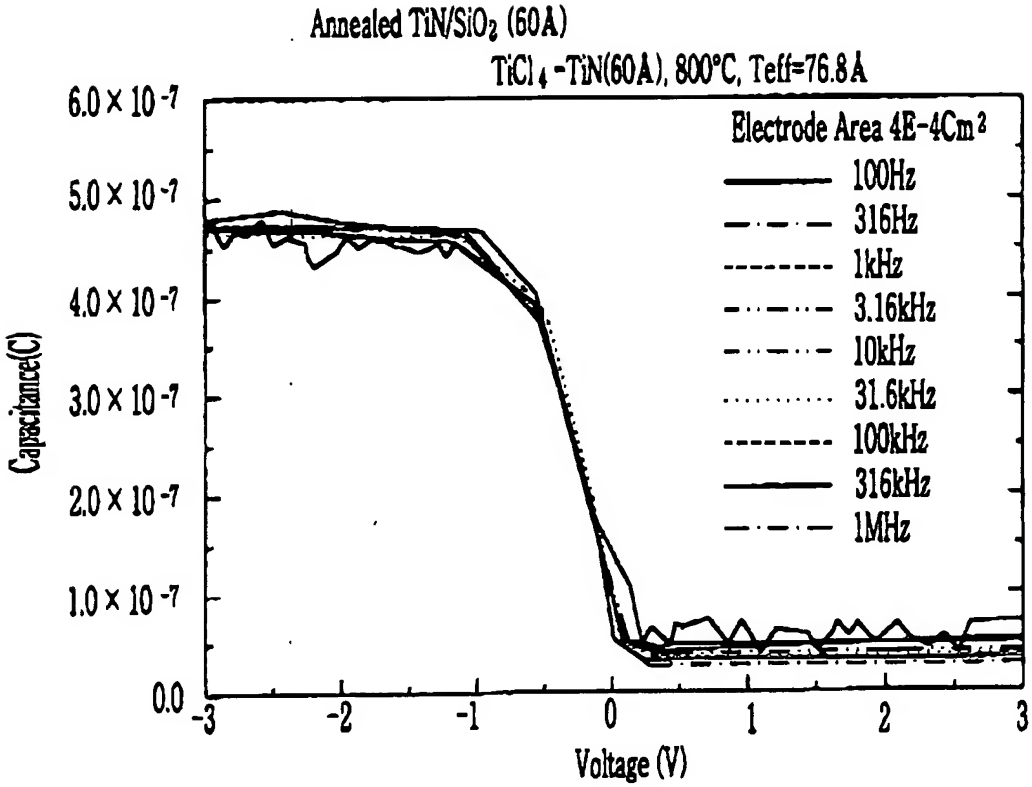


FIG. 3A

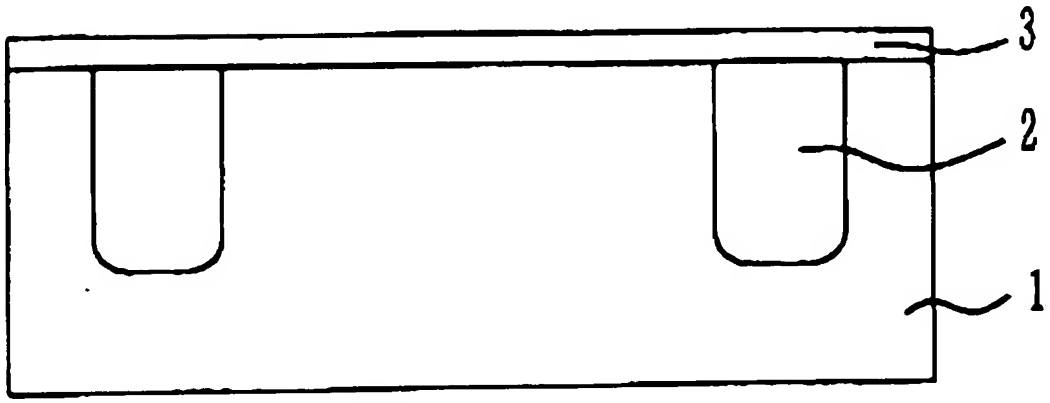


FIG. 3B

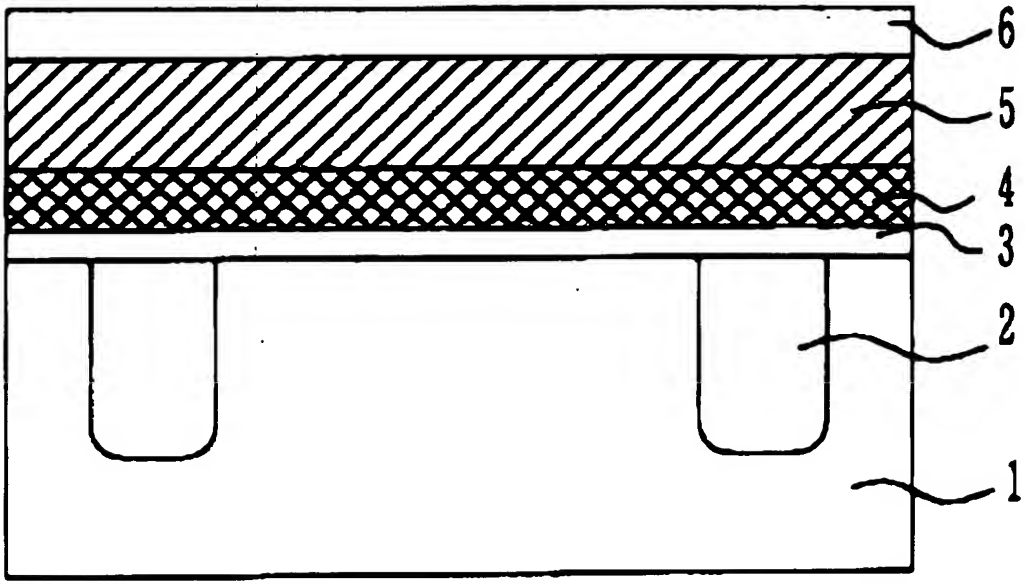


FIG. 3C